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EXAMINER	
ARCOS, CAROLINE H	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/774,178	YEUNG ET AL.	
	Examiner	Art Unit	
	CAROLINE ARCOS	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7,10-15,19,39-41 and 43-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4, 7, 10, 11-15, 19, 39-41, and 44-50 are pending for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 7, 11, 12-14, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lanzafame et al. (US 7006511 B2), in view of Horden (US 5812860 A), and further in view of Zaccarin et al. (US 2003/0115428 A1).

4. As per claim 1, Lanzafame teaches the invention substantially as claimed including a method, comprising:

monitoring a state of an application running in a system, including monitoring one or more buffers associated with the application (abs; col. 1, lines 50-65; col. 2, lines 1-32)

monitoring a machine state of the system, including determining the availability of configurable hardware components in the system, wherein the configurable hardware components include at least a buffer(abs; col. 1, lines 50-65; col. 2, lines 1-32) ;

dynamically adjusting the buffer size based at least on the state of the application

and the state of the one or more threads in the system(abs; col. 1, lines 50-65; col. 2, lines 1-32);

5. Lanzafame does not explicitly teach coordinating dispatch of one or more threads in the system at least in part to increase execution overlap, wherein at least one thread is associated with the application;

dynamically adjusting one or more of the frequency or the voltage applied to the processor based at least on the state of the application and the state of the one or more threads; and the configurable hardware components include at least a processor.

6. However, Horden teaches dynamically adjusting one or more of the frequency or the voltage applied to the processor based at least on the state of the application and the state of the one or more threads; and the configurable hardware components include at least a processor (abs.; col. 3, lines 35-col. 4, lines 1-67).

7. It would be obvious to one of ordinary skill in the art at the time the invention was made to combine Lanzafame and Horden because of Horden teaching of dynamically adjusting one or more of the frequency or the voltage applied to the processor based at least on the state of the application and the state of the one or more threads; and the configurable hardware components include at least a processor would in crease resources to be managed and controlled in the system and gives more control over the hardware resources in the system.

8. The combined teaching does not explicitly teach coordinating dispatch of one or more threads in the system at least in part to increase execution overlap, wherein at least one thread is associated with the application.

9. However, Zaccarin teaches coordinating dispatch of one or more threads in the system at least in part to increase execution overlap, wherein at least one thread is associated with the application (par. [0013], lines 5-7; par. [0014], lines 1-23; par. [0021]).

10. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine from Lanzafame, Horden and Zaccarin because Zaccarin teaching of controlling the transmission rate of data (threads) associated with the application would improve Paul system performance and efficiency in reducing overall power consumption and improve system resource usage.

11. As per claim 7, Zaccarin teaches the configurable hardware components include one or more processors, hardware buffers, memory, cache, arithmetic logic unit (ALU), and registers in the system (par. [0019], lines 4-9; par. [0021], lines 9-13).

12. As per claim 11, Zaccarin teaches said monitoring the one or more buffers associated with the application includes monitoring buffer fullness levels of the one or more buffers (par. [0013], lines 11-12; par. [0014], lines 10-23; par. [0015], lines 8-16; par. [0016], lines 10-12; par. [0018]).

13. As per claim 12, Zaccarin teaches said monitoring the buffer fullness levels includes, for each buffer associated with the application, comparing a buffer level with predetermined buffer fullness levels, wherein the predetermined buffer fullness levels include a high level mark and a low level mark (par. [0015], lines 8-16; Par. [0017]; par. [0018]).

14. As per claim 13, Zaccarin teaches said comparing is to determine buffer overflow and buffer underflow conditions (par. [0015], lines 4-16; par. [0017], lines 4-15).

15. As per claim 14, it is the computer readable storage medium of the method claim 1. Therefore, it is rejected under the same rational.

16. As per claim 19, Zaccarin teaches said monitoring the buffer fullness levels includes, for each buffer associated with the application, comparing a buffer level with predetermined buffer fullness levels, wherein the predetermined buffer fullness levels include a high level mark and a low level mark (par. [0013], lines 11-12; par. [0014], lines 10-23; par. [0015], lines 8-16; par. [0016], lines 10-12; par. [0017]; par. [0018]).

17. Claims 2-4 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lanzafame et al. (US 7006511 B2), in view of Horden (US 5812860 A), in view of Zaccarin et al. (US 2003/0115428 A1).and further in view of Kling et al. (US 6,662,203 B1).

18. As per claim 2, Zaccarin teaches a thread includes one or more activities (par. [0021], lines 1-20).

19. The combined teaching of Lanzafame , Horden and Zaccarin does not explicitly teach that a thread includes one or more activities, and wherein said controlling the dispatch of the one or more threads in the system includes assessing execution readiness of the one or more activities.

20. However, Kling teaches a thread includes one or more activities, and wherein said controlling the dispatch of the one or more threads in the system includes assessing execution readiness of the one or more activities (abs; col. 9, lines 35-67; col. 10, lines 1-9; fig. 5, 77).

21. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Lanzafame , Horden and Zaccarin and kling because Kling teaching of accessing readiness of the one or more activities improve system dispatching techniques and increase efficiency in dispatching technique of the system since one would only be dispatching ready activities only which improve the performance of the system.

22. As per claim 3, Kling teaches said controlling the dispatch of the one or more threads in the system includes delaying a ready-to-be-dispatched activity from being dispatched (abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col. 3, lines 58-col. 4, lines 1-24; col. 9, lines 38-col. 10, lines 1-15).

23. As per claim 4, Zaccarin teaches the first and second activities are from one or more applications (par. [0012]; par. [0021]).

24. The combined teaching of Lanzafame , Horden and Zaccarin does not explicitly teach that a first activity is delayed from being dispatched to wait for a second activity to be ready so that both the first and second activities can be dispatched together.

25. However, Kling teaches a first activity is delayed from being dispatched to wait for a second activity to be ready so that both the first and second activities can be dispatched together.

26. As per claim 15, it is the computer readable medium of the method claim 3. Therefore it is rejected under the same rational.

27. Claim 10 rejected under 35 U.S.C. 103(a) as being unpatentable over Lanzafame et al. (US 7006511 B2), in view of Horden (US 5812860 A), and in view of Zaccarin et al. (US 2003/0115428 A1) as applied to claim 7 above and further in view of Jain et al. (US 2002/0188884 A 1).

50. As per claim 10, the combined teaching of Lanzafame , Horden and Zaccarin does not explicitly teach that said increasing or decreasing the resources in the system includes powering on or powering off at least a portion of circuitry in the system.

28. However, Jain teaches said increasing or decreasing the resources in the system includes powering on or powering off at least a portion of circuitry in the system (par. [0040]; claim 1).

29. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Lanzafame , Horden , Zaccarin and Jain because Jain teaching of said increasing or decreasing the resources in the system includes powering on or powering off at least a portion of circuitry in the system would improve system energy consumption and increase efficiency.

30. Claims 48-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaccarin et al. (US 2003/0115428 A1) and in view of Kling et al. (US 6,662,203 B1).

31. As per claim 48. Zaccarin teaches an apparatus, comprising:
logic to monitor states of an application running in a system, the states of the application including buffer fullness levels of one or more buffers used by the application (abs., lines 9-12; col. 2, lines 29-32; col. 2, lines 62-66; col. 12, lines 18-28; par. [0015], lines 4-16; par. [0017], lines 4-15);

logic to adjust resources available in the system depending on the state of the application and/or the states of the one or more threads in the system (par. [0014]; par. [0015]; par. [0016]); and a memory to store the logic (par. [0024]).

32. Zaccarin does not explicitly teach logic to monitor states of one or more threads in the system for execution readiness. However, Kling teaches logic to monitor states of one or more threads in the system for execution readiness (abs; col. 9, lines 35-67; col. 10, lines 1-9; fig. 5, 77).

33. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin and Kling because Kling teaching of monitoring the execution readiness of one or more thread would improve Zaccarin system performance and dispatching techniques by knowing that one or more threads are ready to be executed, one would be able to take the steps necessary to dispatch them.

34. As per claim 49, Kling teach logic to change the execution readiness of a thread from a ready state to a queued state (abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col. 3, lines 58-col. 4, lines 1-24; col. 9, lines 38-col. 10, lines 1-15; fig. 5).

35. The combined teaching of Zaccarin and Kling does not explicitly teach that the change in state is when it is determined that there is no other thread running or ready to be dispatched.

36. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude from the combined teaching and especially Kling teaching that the ready threads are moved to wait queue until the batch is complete to be dispatched so it would have been obvious that the first thread in the ready queue is moved to the wait queue until

other ready threads becomes ready and join the first thread in the wait queue, when they will be dispatched.

37. As per claim 50, Zaccarin teaches that the logic to adjust the available resources in the system includes logic to determine if the buffer fullness levels of one or more buffers are in a critical stage (par.[0015]; par. [0017]).

38. Claims 39 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaccarin et al. (US 2003/0115428 A1), in view of Lanzafame et al. (US 7006511 B2), and further in view of Horden (US 5812860 A).

39. As per claim 39, Zaccarin teaches a system, comprising:
a memory (fig. 4; 42); processor (fig. 4, 56); monitor a state of an application running in a system, wherein said monitoring the state of the application includes monitoring buffer fullness levels of one or more buffers associated with the application (par. [0013]; par. [0014]
control dispatch of one or more threads in the system, and wherein at least one thread in the system is associated with the application; and manage resources in the system based at least on the state of the application and the state of the one or more threads in the system (par. [0014]; par. [0015]; par. [0021]).
a memory to store data and instructions (par. [0024]).

coordinate dispatch of one or more threads in the system at least in part to increase execution overlap~ wherein at least one thread is associated with the application (par. [0012];

par. [0021]).

40. Zakarin does not explicitly teach a processor coupled to said memory on a bus, said processor operable to perform
instructions, said processor comprising:
a bus unit to receive a sequence of instructions from said memory;
an execution unit coupled to said bus unit, said execution unit to execute said sequence of instructions.

monitoring a machine state of the system including determining the availability of configurable hardware components in the system wherein the configurable hardware components include at least a buffer; dynamically adjusting the buffer size based at least on the state of the application and the state of the one or more threads in the system

dynamically adjust one or more of the frequency or the voltage applied to the processor based at least on the state of the application and the state of the one or more threads; and wherein the configurable hardware components include at least a processor

41. However, Lanzafame teaches a processor coupled to said memory on a bus, said processor operable to perform
instructions, said processor comprising:
a bus unit to receive a sequence of instructions from said memory;
an execution unit coupled to said bus unit, said execution unit to execute said sequence of instructions.

monitoring a machine state of the system including determining the availability of configurable hardware components in the system wherein the configurable hardware components include at least a buffer; dynamically adjusting the buffer size based at least on the state of the application and the state of the one or more threads in the system (abs; col. 1, lines 50-65; col. 2, lines 1-32).

42. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin and Lanzafame because Lanzafame teaching would improve managing and controlling system resources.

43. the combined teaching of Zaccarina and Lanzafame does not explicitly teach coordinating dispatch of one or more threads in the system at least in part to increase execution overlap, wherein at least one thread is associated with the application;

dynamically adjusting one or more of the frequency or the voltage applied to the processor based at least on the state of the application and the state of the one or more threads; and the configurable hardware components include at least a processor.

44. However, Horden teaches dynamically adjusting one or more of the frequency or the voltage applied to the processor based at least on the state of the application and the state of the one or more threads; and the configurable hardware components include at least a processor (abs.; col. 3, lines 35-col. 4, lines 1-67).

45. It would be obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin, Lanzafame and Horden because of Horden teaching of dynamically adjusting one or more of the frequency or the voltage applied to the processor based at least on the state of the application and the state of the one or more threads; and the configurable hardware components include at least a processor would in crease resources to be managed and controlled in the system and gives more control over the hardware resources in the system.

46. As per claim 41, Zaccarin teaches that said execution unit to monitor a machine state of the system, wherein said monitoring the machine state includes: increasing or decreasing the configurable hardware components available in the system based on the state of the application and the state of the one or more threads in the system (par. [0014]; par. [0015]; par. [0017]).

47. Zaccarin does not explicitly teach determining resources available in the system. However, Lanzafame teaches determining resources available in the system (abs; col. 1, lines 50-65; col. 2, lines 1-32).

48. Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zaccarin et al. (US 2003/0115428 A1), in view of Lanzafame et al. (US 7006511 B2), in view of Horden (US 5812860 A) and further in view of Kling et al. (US 6,662,203 B1).

49. As per claim 40, the combined teaching of Zaccarin, Lanzafame and Horden does not explicitly teach that said controlling the dispatch of the one or more threads in the system includes delaying a ready- to-be-dispatched thread from being dispatched.

50. However, Kling teaches said controlling the dispatch of the one or more threads in the system includes delaying a ready-to-be-dispatched thread from being dispatched(abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col. 3, lines 58-col. 4, lines 1-24; col. 9, lines 38-col. 10, lines 1-15; fig. 5).

51. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin, Lanzafame , Horden and kling since Kling teaching of delaying a ready-to-be- dispatched thread from being dispatched would improve system throughput and increase efficiency of system resource usage.

52. Claims 44-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaccarin et al. (US 2003/0115428 A1), in view of Kling et al. (US 6,662,203 B1) and further in view of Peter et al. (US 5,668,993).

53. As per claim 44, Zaccarin teaches a system, comprising:

processor (fig. 4, 56);

a resource manager coupled to the multi-threading processor (fig. 4);

the resource manager is to monitor states of an application running in the system, the

states of the application including buffer fullness levels of one or more buffers used by the application, wherein the resource manager is to increase or decrease resources available in the system depending on the state of the application and/or the states of the one or more threads in the system (par. [0013]; par. [0014]; par. [0015]; par. [0017]; par. [0021]).

54. Zaccarin does not explicitly teach a multi-threading processor; and the resource manager is to further monitor states of one or more threads in the system for execution readiness.

55. However, kling teaches the resource manager is to further monitor states of one or more threads in the system for execution readiness (abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col. 3, lines 58-col. 4, lines 1-24; col. 9, lines 38-col. 10, lines 1-15; fig. 5).

56. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin and Kling because Kling teaching of monitor states of one or more threads in the system for execution readiness would improve dispatching and scheduling techniques and system performance by monitoring ready thread to dispatch them.

57. The combined teaching does not explicitly teach that the processor is a multi-threaded processor. However, Peter teaches that the processor is multi-threaded processor (col. 5, lines 35-40; col. 9, lines 50-56).

58. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin, kling and Peter because Peter teaching of multithreaded processor would improve system performance and throughput.

59. As per claim 45, Kling teaches that wherein the resource manager is to change the execution readiness of a thread from a ready state to a queued state to increase subsequent thread execution overlap with execution of another thread (col. 2, lines 10-16).

60. As per claim 46, Kling teaches change the execution readiness of a thread from a ready state to a queued state (abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col. 3, lines 58-col. 4, lines 1-24; col. 9, lines 38-col. 10, lines 1-15).

61. The combined teaching of Zaccarin, Kling and Peter does not explicitly teach that the change is to increase subsequent system idle time when there is no thread execution. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude from Kling teaching of batch system and changing from ready to queued state that beside increasing the efficiency in using the system resource, it is increasing subsequent system idle time when there is no thread execution which improve the system throughput by processing the threads in a parallel at once.

62. As per claim 47, Zaccarin teaches the resource manager is to increase or decrease the resources available in the system to avoid buffer underflow or overflow conditions to occur to

the one or more buffers (par. [0013]; par. [0014]; par. [0015]; par. [0017]).

Response to Arguments

63. Applicant's arguments with respect to claim1-4, 7, 10, 11-15, 19, and 39-41 have been considered but are moot in view of the new ground(s) of rejection.

64. Applicant's arguments filed 03/10/2209 have been fully considered but they are not persuasive..

65. Applicant argues the obviousness in claim 49 that change the execution readiness of a thread from a ready state to a queued state when there are no other threads to be dispatched.

66. Examiner respectfully disagree with the applicant that it is known to one of ordinary skill in the art to change the thread execution from ready to queued when there is no other threads to be dispatched . However, it is well known that that a thread in a ready state, it is in the ready queue state waiting to be dispatched, hence it is not really changing state since it is already in a queue waiting to be dispatched.

Conclusion

67. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

68. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CAROLINE ARCOS whose telephone number is (571)270-3151. The examiner can normally be reached on Monday-Thursday 7:00 AM to 5:30 PM.

69. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

70. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/VAN H NGUYEN/
Primary Examiner, Art Unit 2194

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Examiner, Art Unit 2195